Practical synthesis of various control methods for digitally adjusted DC-DC converters

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Abstract - **This paper aims to present a comparative study of various digital control methods for DC-DC converters. These control methods uses Digital Potentiometers, Digital Analog Converters or filtered DPWM signals connected in the feedback control loop of a DC-DC converter in order to adjust the output voltage of the converter. The synthesis presents different mathematical models for calculating the optimal component values for each type of control, detailing the most common effects of components value variation over the entire output range of the converter. The results from computer-aided simulations and a series of experimental measurements validate each previously presented mathematical model. In conclusion, the control methods comparison offers some practical advises about the linearity, resolution, code efficiency in real applications.**

I. INTRODUCTION

Applying digital control techniques to switch mode power supplies is interesting because it adds several advantages such as flexibility, precision etc. with the use of software control. However, pure digital control has also disadvantages such as bandwidth, switching frequency, cost, etc. [1]. Our approach is to describe the hybrid methods by using the good dynamic performances of an analog controller and adding the flexibility of controlling the output voltage with a simple MCU unit. This paper presents three different methods each having advantages and disadvantages. One of the advantages of this hybrid method is the possibility of adding an external control loop with a narrower loop bandwidth in order to counteract temperature effect, offset and aging of a pure analog power supply. It is also possible to add power and data management functions such as monitoring, on-off control, power-up sequencing, customizable soft start times etc. The external loop bandwidth depends on typical digital control parameters such as instruction cycle speed of the MCU, A/D conversion time, filtering. In the DAC, and Digital Potentiometer based methods the transmission speed of serial communication (typically I2C or SPI) between the MCU and DAC or MCU and Digital Potentiometer narrows the control loop bandwidth as the main delay factor in the feedback loop. In the DPWM method, this loop delay is considerably less, since it is dependent only by the instruction cycle speed of the MCU (when the duty cycle value in the DPWM generating register is changed) and the delay introduced by the output filter that filters out the AC component of the DPWM signal. The main experimental application, a digitally controlled DC-DC converter, is based on a low-power, high-performance USB capable, 8-bit RISC MCU (PIC18F46J50) [11] and on a high efficiency, synchronous, 4-switch buck-boost controller (LTC3780) [7], [8]. The input voltage of the converter is set to +12V, supplied by a laboratory grade PSU.

An earlier studied article [4] highlights basic equations for adjusting the output voltage of a DC-DC converter but without calculating the parameters for a desired output voltage range. Based on this article statement we try to develop further results.

The output voltage range for the experimental DC-DC converter is set between 5V to 25V. Each investigated control method has 8-bit resolution. The optimal component values are calculated based on this given resolution parameter in order to validate the mathematical models by the experimental results.

An external control loop can compensate the differences between the simulated and experimental results. The main principles of an external control loop design described in Buso's article [5] can be applied for the methods presented in this paper.

II. DIGITALLY ADJUSTABLE DC-DC CONVERTERS

A. Control method using a Digital Analog Converter

Fig.1 presents the block schematic of a DAC based adjustable DC-DC converter. The DAC unit connects through an SPI bus to a simple 8-bit RISC based MCU. The MCU controls the DAC's output voltage using an algorithm, influencing the overall output of the DC-DC converter. The experimental circuit uses the DAC5573, a quad 8-bit low power DAC chip [9]. DAC circuit architectures and theory of operation is available in several referenced books [4], [12], [13], [15] that discusses exhaustively the different types of DACs, but detailing them is out of the scope of this paper.

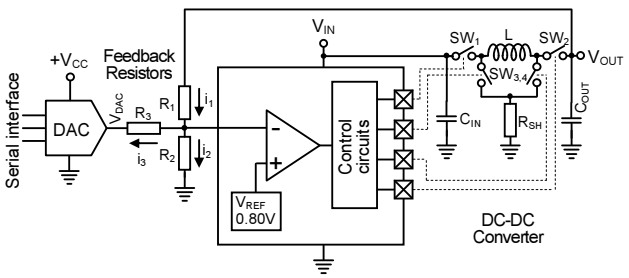

Fig. 1. DAC based control circuit

Applying Kirchhoff's laws for voltage and currents in the above circuit (Fig.1), we have:

$$i_1 = i_2 + i_3 \quad (1)$$

$$i_2 = \frac{V_{REF}}{R_2} \quad (2)$$

$$i_3 = \frac{V_{REF} - V_{DAC}}{R_3} \quad (3)$$

$$V_{OUT} = i_1 \cdot R_1 + V_{REF} \quad (4)$$

where i_1, i_2 and i_3 are the currents flowing through the R_1, R2 and R_3 resistors respectively, V_{REF} is the internal reference of the DC-DC converter, and V_{OUT} is the converter's output voltage.

Substituting eq.2 and eq.3 in eq.1, and substituting eq.1 in eq.4 results eq.5:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + \left(V_{REF} - V_{DAC}\right) \cdot \frac{R_1}{R_3} \quad (5)$$

In addition, the value of R3 is expressed using eq.5:

$$R_3 = \frac{\left(V_{REF} - V_{DAC}\right) \cdot R_1}{V_{OUT} - V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)} \quad (6)$$

The next step establishes the output voltage range, defined by the minimum and maximum allowable voltages, generated by the DAC converter, in order to calculate the optimal values of the resistors R_1, R_2 and R_3 (Fig.1.). To achieve the desired settings we can write the following equations based on eq.5.

$$V_{OUTMIN} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + \left(V_{REF} - V_{DACMAX}\right) \cdot \frac{R_1}{R_3} \quad (7)$$

$$V_{OUTMAX} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + \left(V_{REF} - V_{DACMIN}\right) \cdot \frac{R_1}{R_3} \quad (8)$$

Where:

V_{OUTMIN} represents the minimum settable output voltage, V_{OUTMAX} is the maximum settable output voltage, V_{DACMIN} is the minimum value of the DAC converter output, and finally the V_{DACMAX} component is the maximum value of the DAC converter output.

In order to obtain the optimal values for the components and given eq. 7 and eq.8, we replace the extreme values of V_{DAC} and V_{OUT} in eq.6 as following:

$$\frac{V_{REF} - V_{DACMIN}}{V_{OUTMAX} - V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)} = \frac{V_{REF} - V_{DACMAX}}{V_{OUTMIN} - V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)} \quad (9)$$

Defining K_1 invariable:

$$K_1 = \frac{V_{REF} - V_{DACMAX}}{V_{REF} - V_{DACMIN}} \quad (10)$$

we obtain:

$$R_2 = V_{REF} \cdot R_1 \cdot \frac{1 - K_1}{V_{OUTMIN} - V_{REF} - K_1 \cdot \left(V_{OUTMAX} - V_{REF}\right)} \quad (11)$$

The eq.11 has multiple solutions but considering the DC-DC converter circuit maker's opinion, regarding the useful range of R_1, the values for R_2 and R_3 can be easily calculated using eq. 6 and eq.11 for the desired output range.

The simulated results presented in Fig.2 (images a, b, c and d) shows the expected variation of the output voltage by varying the R_3 resistor value at different DAC reference voltages: 1.25V (a), 2.5V (b), 3.3V (c) and 5V (d) respectively. Every image highlights different cases where R_3 resistor taking values around the calculated one, being 90, 95, 100, 105 and 110 percent of the initial value. We observe that the curves are intersecting when V_{REF}=V_{DAC} condition is satisfied and if V_{DACMAX}<$V_{REF,}$ the lower limit of adjustable output from the desired voltage range, does not satisfies. For the experimental buck-boost controller circuit the reference voltage is set to 0.8V.

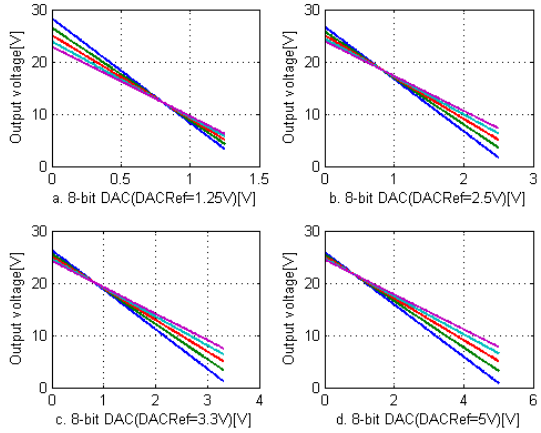

Fig. 2. Effect of DAC references at different R_3

The adjustable DC-DC converter output controlled by a DAC circuit shows 256 samples of the simulated vs. experimental data in Fig.3, measured with an overall linear

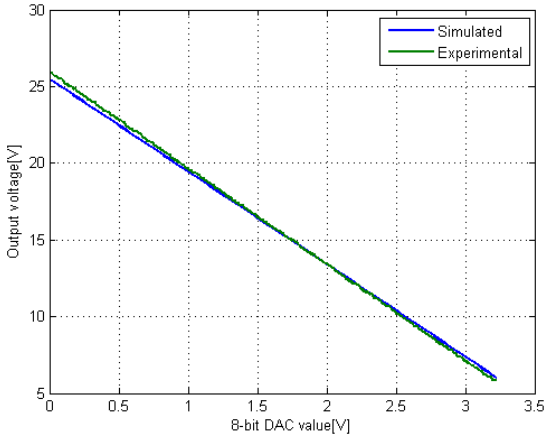

Fig. 3. Simulated vs. Experimental data

characteristic. Some nonlinearity can be introduced by the differential nonlinearity(DNL) of the DAC which could be max +/-0.25LSB for the DAC selected [9].

Fig.4 plots the differences between the simulated and experimental data. This error value is the most highest at the extremes of the defined output voltage range.

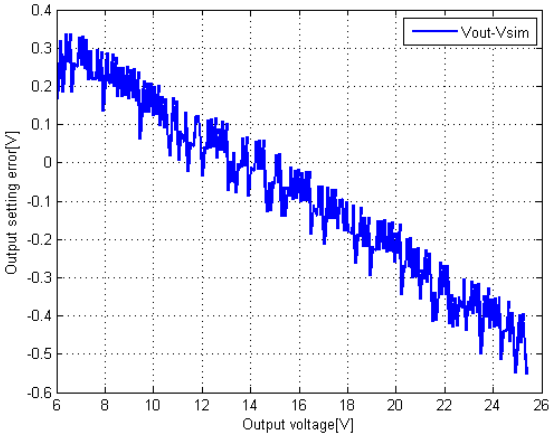

Fig. 4. Error between simulated and experimental data

B. Control method using a Digital Potentiometer

By definition, the digital potentiometer is a digitally controlled electronic circuit (usually through a serial interface like I2C or SPI buses) that mimics the analog functions of a given value potentiometer. The second series of experiment uses the MCP4552, a single channel, I^2C, digital potentiometer, with volatile memory [10].

Fig.5 sketches the digital potentiometer based adjustable DC-DC converter. The same, simple 8-bit RISC architecture

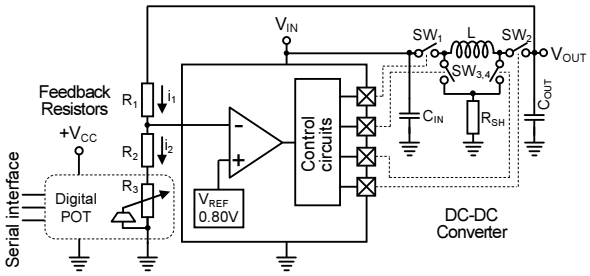

Fig. 5. Digital Potentiometer based control circuit

MCU interfaces the digital potentiometer. The MCU controls the digital potentiometer's resistance value by an algorithm influencing the overall output of the DC-DC converter [14].

Must be noted that many types of digital potentiometers cannot withstand higher voltages than their input power supply, which is usually +3.3V or +5V. This is the reason why the potentiometer cannot reside at the high side portion of the dividing feedback line when the power supply needs to be adjusted at a higher voltage level.

This particular arrangement will introduce a nonlinear characteristic of the output voltage, depending on the digital potentiometer setting, detailed later in this paper.

The most important characteristics of the digital potentiometer are:

- The resistance of the potentiometer, which varies between 0 Ohm and the maximum value specified in the datasheet
- The cursor's self-resistance, which determines the minimum value of potentiometer's resistance
- Number of steps (in other words the resolution of the potentiometer), which can be distributed linearly or logarithmic

The error sources affecting the precision of the current setting are the precision of the digital potentiometer, which has a rather large variation of +/-25%, the cursor's precision, and temperature dependence of the entire circuit. The settings can be stored either volatile or non-volatile, depending on whether the desired values are saved or not in the circuit's internal EEPROM. As soon as the volatile digital potentiometer has power, its resistance value is usually set at the half of the maximum possible value, since its value is not saved in internal memory. A protective mechanism needs to activate in order to ensure that the converter does not output inadmissible voltages due to the nominal setting of the potentiometer. A good method to achieve this performance is to activate the DC-DC converter output only after the desired setting downloads through the potentiometer's communication interface.

Applying again Kirchhoff's laws for voltage and currents for the circuit above, we got:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2 + R_3}\right) \tag{12}$$

The sum of digital potentiometer's resistance R_P together with the cursor's resistance R_C determines the value of R_3.

$$R_3 = R_P + R_C \tag{13}$$

Calculating the optimal values of the components, similar as in the first method, using a DAC, provides the desired output voltage range. After choosing the digital potentiometer circuit, the minimum and maximum possible values of R_P are known, so we obtain eq.14, and eq.15 from eq.12 and eq.13. as they follows:

$$V_{OUTMIN} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2 + R_{PMAX} + R_C}\right) \tag{14}$$

$$V_{OUTMAX} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2 + R_{PMIN} + R_C}\right) \tag{15}$$

After rearranging eq.14, we obtain:

$$R_1 = \frac{\left(V_{OUTMIN} - V_{REF}\right) \cdot \left(R_2 + R_{PMAX} + R_C\right)}{V_{REF}} \tag{16}$$

Replacing the value of R_1 in eq.15 with R_1 value taken from eq.14 and doing the calculations, then rearranging the

components in the given formula, finally we obtained the value of R_2.

$$R_2 = \frac{V_{REF} \cdot (R_{PMIN} - R_{PMAX}) + V_{OUTMIN} \cdot R_{PMAX} - V_{OUTMAX} \cdot R_{PMIN}}{V_{OUTMAX} - V_{OUTMIN}} - R_C \quad (17)$$

Since R_2 value is known, R_1 is easily obtained.

The simulation result in Fig.6 shows the dominant nonlinearity of the characteristics, using a digital potentiometer with resistance of 5KOhm but ranging this value in between a 80-120% domain of the nominal value.

The output resolution shown in Fig.7 emphasizes that the resolution is also nonlinear and it is higher at the higher section of the output voltage domain

Fig. 8 compares the simulated and experimental results for the calculated component values. The difference between the simulated and experimental data shows a nonlinear tendency of the error and points higher error values at superior voltage settings (Fig. 9).

C. Control method using a PWM signal

Most microprocessors integrate digitally controlled PWM outputs. Adjusting the duty cycle value of the DPWM signal controls the average voltage value of the signal applied in the feedback circuit of a DC-DC converter. This voltage should have low AC component value so we apply a low-pass filter to the output of the PWM signal resulting in a simple, digital analog converter circuit.

This method turns out to be the cheapest one, because it does not require other components than those needed to achieve a simple low pass filter (for example, a single resistor and a capacitor easily form a first order low-pass filter). In terms of power consumption and MCU clock frequency, the PWM method is more "expensive" than using a digital potentiometer or a dedicated digital to analog converter.

The following schematic (Fig.10) presents the principles of a DPWM based adjustable DC-DC converter. This time the MCU controls the DPWM signal's frequency and duty cycle. In our experiment, we keep the DPWM signal's frequency constant. By changing the duty-cycle of this signal, the average DC voltage value applied to the analog feedback control loop also changes. The group of R_4, C_1 forms the low-pass filter and the R_3 resistor role is to smooth the effect of capacitor C_1 over the dynamic performances of the DC-DC converter's inner control loop.

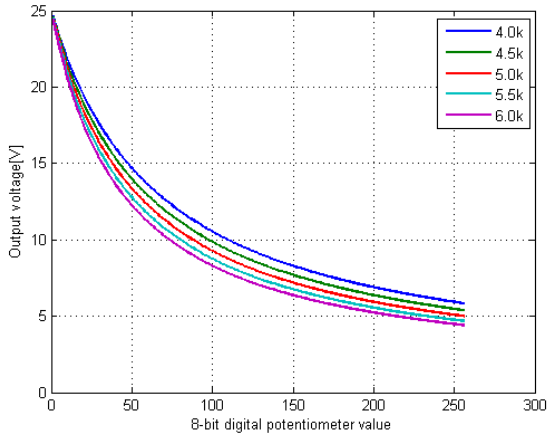

Fig. 6. Output voltage depending potentiometer value

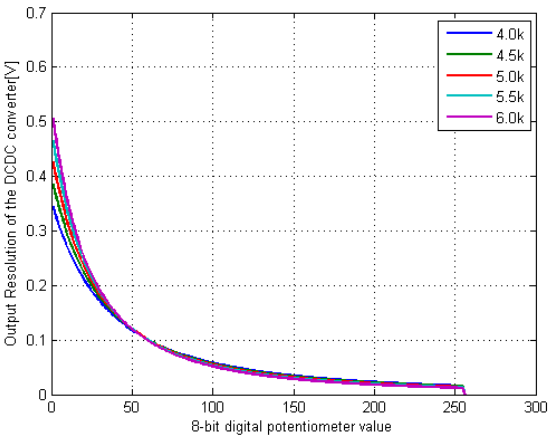

Fig. 7. Output resolution of the DCDC converter

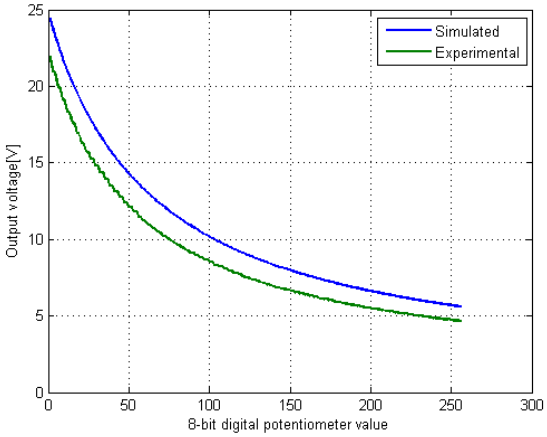

Fig. 8. Simulated and experimental data

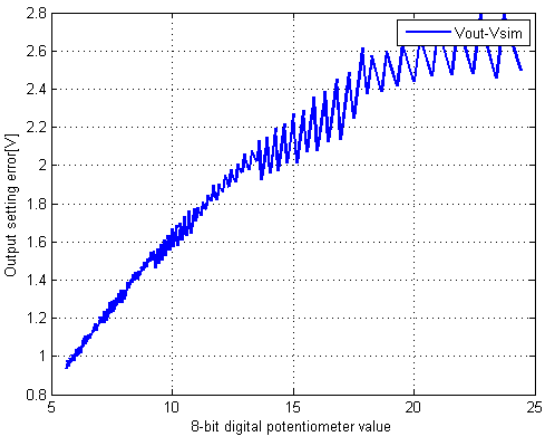

Fig. 9. Error between simulated and experimental data

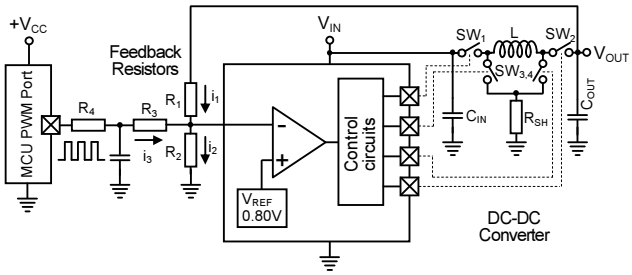

Fig. 10. DPWM based control circuit

DPWM outputs are imprecise by their nature because they are inherently dependent on digital low and high logic levels generated by the PWM controller that varies with the supply voltage variation and other system parameters. Eq. 18 defines the output voltage of the DPWM at a given moment in time as following:

$$V_{PWMt}=f(V_L,V_H, f_{PWM}, D, t) \quad (18)$$

Where V_L represents the minimum DC voltage generated by the DPWM output, V_H is the maximum DC voltage generated by the DPWM output, f_{PWM} means the frequency of the DPWM signal, D is the duty cycle of the DPWM signal and finally, t is the considered moment in time.

Since V_L and V_H can have relatively large variations, this method is mainly used in a closed loop where is possible to measure the output and adjust the PWM parameters to achieve the desired output voltage.

The simulated results in Fig.11 shows the influence of logic high level when logic low level is at 0V and Fig.12 points the influence of logic low level when logic high level is set to 3.3V.

The formula for the output voltage writes similarly to the DAC control method using the same notations:

$$V_{OUT} = V_{REF} \cdot \left(1+\frac{R_1}{R_2}\right) + \left(V_{REF} - V_{PWM}\right) \cdot \frac{R_1}{R_3+R_4} \quad (19)$$

Where

$$V_{PWM} = D \cdot V_H + (1-D) \cdot V_L \quad (20)$$

knowing that V_H and V_L are the digital high and low logic level value of the DPWM signal.

The optimal resistor values for R_1, R_2 and R_3 in series with R_4 calculates in a similar way as presented earlier in the DAC based control method.

Having N bit resolution the following relationship needs to be fulfilled:

$$f_{PWM} \le \frac{f_{instr}}{2^N} \quad (21)$$

where f_{instr} is the frequency of the instruction cycle and N is the resolution to achieve.

In case of high resolution, high frequency counter based DPWM solution is needed the use of Hybrid DPWMs is preferred [3]. The experimental circuit includes an 8-bit RISC MCU running on 48MHz oscillator frequency to fulfill USB requirements. The given instruction cycle frequency is 12MHz, which determines the highest PWM frequency used for the 8-bit PWM based DAC resolution to be 46.875KHz in accordance with eq.21. The higher the PWM frequency is, the easier is to filter out the ripple with a simple low pass filter. Ripple voltage should be filtered out as much as possible, so it does not interfere with the internal control loop of the DC-DC converter.

Choosing a ripple size of 1LSB, we have:

$$R_4 \cdot C_1 = \frac{2^{N-2}}{f_{PWM}} \quad (22)$$

By choosing a suitable value for C_1 the value of R_4 can be calculated by rearranging eq.22. The value of R_3 connected in series with R_4 is also known from previous relations, so the value of R_3 is easily calculated.

The ripple voltage is expressed as:

$$V_{ripple} = \left(V_H - V_L\right) \cdot \frac{1-e^{-\frac{T}{2R_4C_1}}}{1+e^{-\frac{T}{2R_4C_1}}} \quad (23)$$

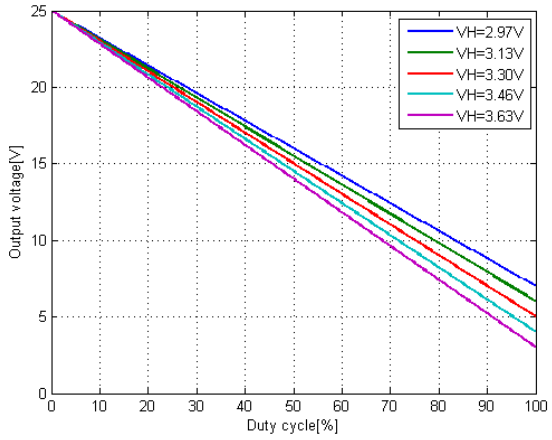

Fig. 11. The effect of V_H level when V_L=0V

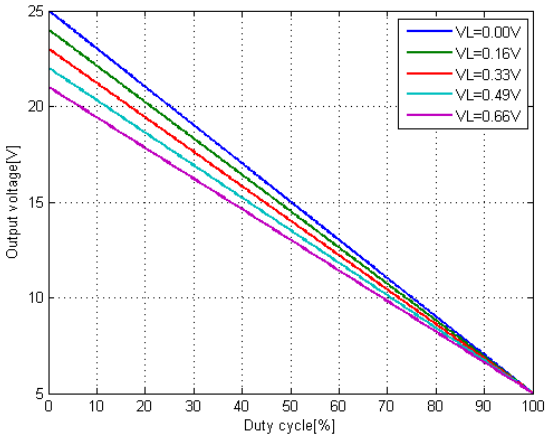

Fig. 12. The effect of V_L level when V_H=3.3V

where T is the PWM period. The ripple is also equal with 1LSB step of the PWM based DAC converter:

$$V_{ripple} = \frac{(V_H - V_L)}{2^N} \quad (24)$$

After performing the necessary calculations the obtained values are as follows:

R_1=30KOhm, R_2=1.24KOhm, R_3=3.58KOhm, R_4=1.36KOhm, C_1=1uF, f_{PWM}=46.875KHz and V_{ripple}=12.9mV.

Trying to use standard resistor values for practical implementation so we get:

R_1=30KOhm, R_2=1.2KOhm, R_3=3.6KOhm, R_4=1.2KOhm, C_1=1uF. After we re-simulate with these data, the ripple value gives V_{ripple}=14.7mV.

The simulation results in Fig.13 shows the effect of the capacitor value C_1 on the ripple voltage with +/-5 - 10% deviation from the standard value.

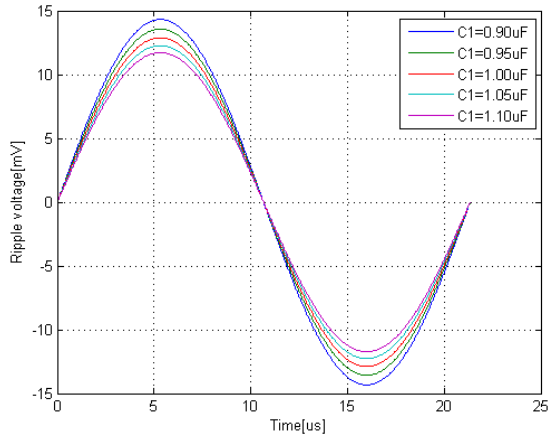

Fig. 13. The ripple voltage on C1 depending its value

The experimental results shown in Fig.14 represents the relationship between the DPWM signal and the resulted ripple and output voltage, where CH1 is the DPWM signal, CH2 is the ripple on C_1 capacitor and CH3 is the resulting output voltage of the DCDC converter. The DPWM signal duty cycle is set at 50%.

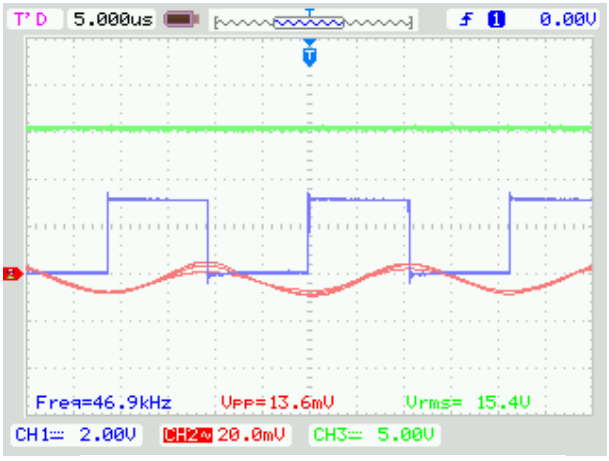

Fig. 14. The measured ripple with 50% duty of DPWM

The following simulated vs. experimental output characteristic of the controlled DC-DC converter (Fig.15) shows a linear characteristic similar as presented for the DAC based control method.

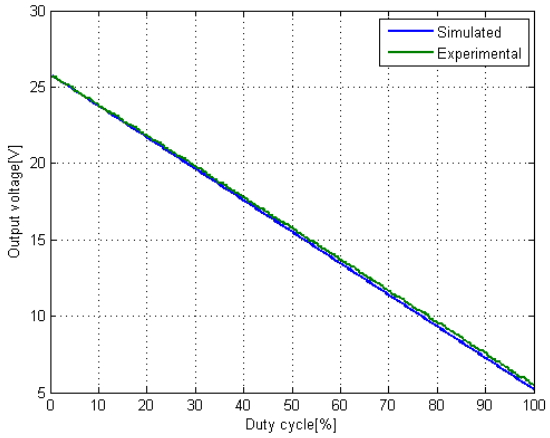

Fig. 15. Simulated vs. experimental

The error between simulated and experimental data (Fig.16) highlights that the differences are bigger at lower voltages indicating that V_H is below the expected 3.3V, measuring only 3.22V, which confirms the simulation results

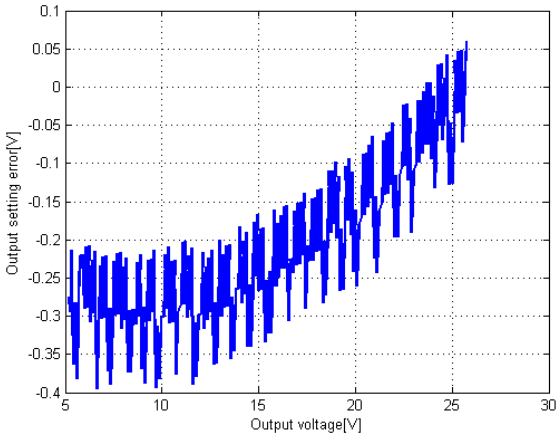

Fig. 16. Error between simulated and experimental data

presented in Fig.11. The simulation in this figure shows that when V_H is lower than the ideal one, the output voltage gets higher and the differences between the ideal and real values are bigger at low voltages.

III. CONCLUSION

The current trend in configurable DC-DC converters clearly points that the output voltage adjustment is a preferred feature for both high and mid end range units. The detailed methods explains the relative easiness to migrate an existing, good behaving analog converter frontend design to an

adjustable DC-DC converter by adding a few extra digital components that adds more flexibility and control to the pure analog solution.

At the final words, the paper tries to summarize the good and the bad of each of the presented control methods resulting in a comparative table concerning different point of views like output voltage resolution, digital resolution, accuracy, robustness, power consumption, price, etc. Further investigation should be performed on how these methods influence the dynamic response of the power supply when using different inner analog voltage or current control loops.

TABLE I

	DAC	Digital Pot.	DPWM
Digital resolution	High	Medium	Low(Oscilla-tor freq. dependent)
Linearity	yes	no	yes
Code execution speed	Medium	Medium	High
Power consumption	Low	Medium	High
Output voltage resolution	Medium	High resolution at low voltages. Low resolution at high voltages.	Medium
Accuracy	High	Low	Medium
Price	Low	Medium	High

The main advantage of the presented solutions over an analogue equivalent is the added flexibility, control and power management capability that a digital solution offers. The resolution of the output converter can be easily extended by changing the added components value for DAC and potentiometer based solutions or by using a higher resolution DPWM signal. An external digital control loop allows for compensation of errors by either using an onboard A/D converter or an external one.

The main disadvantage of these solutions is that dynamically adjusting the output voltage introduces a perturbation in the analog voltage control loop since the analog controller sees the voltage change at the reference voltage comparator as a sudden voltage change at the output, which interacts with the load-regulation control loop of the analog controller. In order to determine the highest voltage step applicable in case of using this solution for an external closed-loop control that dynamically changes the output voltage, the exact model of the internal control loop must be available. Even if there are experimental possibilities to determine the internal loop model, this could be inaccurate or cumbersome to validate. This is why the practical implementation could be difficult in some cases since these methods could influence the dynamic response of the power supply when used in closed loop control and should be applied with care.

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